than the first voltage;

a data storage circuit for storing therein the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal;

a data bus for transmitting the image signal from the data storage circuit; and

a voltage select circuit for selecting from the image signal on the data bus a voltage used to drive the liquid crystal display panel and then outputting the voltage selected.

5. A liquid crystal display device having a liquid crystal display element, a plurality of cascade-connected liquid crystal drive circuits, and a plurality of signal lines formed over an edge portion of the liquid crystal display panel for transmitting a signal between any two of the drive circuits, wherein each of the liquid crystal drive circuits comprises:

a data input terminal connected with one of the signal lines to receive an image signal being input thereto;

a clock compensation circuit for inputting an external clock and outputting an internal clock, the internal clock having a first period for outputting a first voltage and a second period for outputting a second voltage;

a data latch circuit for taking thereto the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock;

a data bus for transmitting the image signal from the data latch circuit;

a voltage output circuit for outputting a voltage selected from the image signal on the data bus to the liquid crystal display element; and

a data output circuit for outputting the image signal on the data bus to a subsequent liquid crystal drive circuit, wherein

the clock compensation circuit corrects a duty ratio deviation from the external clock signal.

Please add the following new claims:

9. The liquid crystal display device as claimed in Claim 1, wherein the duty ratio deviation from the external clock signal is caused by at least one of an internal characteristic of the

respective drive circuit and a factor on the signal lines.

10. The liquid crystal display device as claimed in Claim 1, wherein the internal clock signal generated by the clock compensation circuit has a duty ratio of 50%.

11. The liquid crystal display device as claimed in Claim 5, wherein the duty ratio deviation from the external clock signal is caused by at least one of an internal characteristic of the respective drive circuit and a factor on the signal lines.

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12. The liquid crystal display device as claimed in Claim 5, wherein the internal clock signal generated by the clock compensation circuit has a duty ratio of 50%.